Experienced-resume

Name: **XXXXXXXX**

Key Expertise:

6.9 Years of hands-on experience executing projects from Netlist to GDSII using Cadence, Synopsys and Mentor tools.

Experience Summary

- Currently working as a Senior Engineer in Larsen & Toubro Technology Services Limited, Chennai from Jan 2014 to till date.
- Worked as Senior Engineer in Larsen & Toubro Infotech Limited, Chennai from Aug 2011 to Dec 2013.
- Worked as Physical Design Engineer in Wipro Technologies Ltd from Aug 2007 to Aug 2011.

Work Summary

- Good experience in Netlist to GDSII of Integrated circuit design flow (P&R, STA, Power analysis and Physical verification)
- Worked on technologies from 180nm to 28nm.
- Knowledge in porting of chip from specific tools to Cadence Virtuoso including Technology file creation etc.
- Worked with low power chips.
- Worked in both flat and hierarchical designs.
- Very good expertise in Physical verification including DRC,LVS, antenna and Lithography checks
- Have done five full chip tape-outs
- Good written and oral communication skills.

Tools skill-set

Place and Route	ICC, EDI (SOCE)
Extraction, STA	QRC, PrimeTime, ETS
Power analysis, SI	EPS, Celtic
Custom Layout	Virtuoso, Lavis
Physical Verification	Calibre

Project Details

Project 1:

		Duration	2 Months

Project Name	USB Device		
		Team Size	3

Name: **XXXXXXXX**

Description	This project was a block-level design implemented in TSMC 28nm HPM process. The block was around 300K gates. The frequency of operation is 125MHz.
Role & Contribution	**Role:** Place & Route **Description & Challenges :** • 4 clock domains for functional mode and single clock-domain for DFT mode. • The design included 12 corners for functional and DFT modes. • Rectilinear floorplan with lots of congestion and utilization of around 80%. • Highly congested design where macro placement played a key role • Timing closure across different corners with signoff tools.
Technologies	TSMC 28nm HPM
Tools	IC compiler
Key Achievements	Quick Turn-around time.

Project 2:

Project Name	Mixed Signal Project	Duration	6 Months
		Team Size	3
Description	OY93 is a block-level design implemented in customer foundry 180nm Generic Superb. The design was very congested and the number of metal layers used for signal routing was only 3. There were also few constraints on the clock buffers and hence they had to be custom placed near the clock ports to meet the delay and timing. BN05 is a block-level design implemented in TSMC 130nm. This design had a very irregular die size. It was in an amoeba shape and hence timing closure, antenna fixing and DRC fixing was a challenge BN02 is a block-level design implemented in TSMC 130nm. It was an ECO project with Base layer already done. It was a highly congested design. The design had a very challenging task as it was both routing and placement congested. The numbers of diodes used were very less and hence working on		

Name: **XXXXXXXX**

	antenna issues was a challenge.
	Role: P&R, Physical Verification **Description & Challenges :** • Netlist to GDSII flow including Place & Route, and Physical

Role& Contribution	verification. • Congested floorplan with only 3 metal routing layers • All designs were implemented as Analog Top flow, where the digital floorplan was dictated by the Analog Macro placement. • Manual Resolution of Antenna issues and re-routing manually due to huge congestion. • Very quick turn-around time. • Projects were executed in parallel and design teams sitting across geographies.
Technologies	180nm with 3 metal routing layers
Tools	EDI, Calibre
Key Achievements	Very quick-turn around time and lots of customer appreciation.

Project 3:

Project Name	DFE	Duration	7 Months
		Team Size	12
Description	DFE is a Femto cell design implemented in 28nm with 5 timing corners. The full-chip gate-count of this design was 0.8 billion Gates. The chip had 20 hierarchical blocks		
Role& Contribution	**Role:** Place & Route, Power Clean-up and Physical verification **Description & Challenges :** • Block level Power clean-up of different blocks in the chip. Power clean up activity involved checking for robustness of the power structure and the integrity of them with respective to the full chip power structure.		

Name: **XXXXXXXX**

	• Merged all the partitions using the platform DEF. • There was no sign-off flow for PV during initial stages of the project. Defined the methodology and the flow to be followed for LVS, DRC and MRC.
Technologies	TSMC 28nm HP
Tools	SOC Encounter, Virtuoso, Calibre
Key Achievements	Quick Turn-around time

Project 4:

Project Name	Hawk	Duration	4 Months
		Team Size	4
Description	Hawk was a block-level design implemented in TSMC 65nm Generic Superb process using the Unified Power format (UPF) flow. The gate-count of the block was around 1.5M gates with 2 power domains namely always ON and power-shut off. The design included isolation cells, level shifters, retention flops and power switches. The frequency of operation is 450MHz.		
Role& Contribution	**Role:** Place & Route, Physical Verification **Description & Challenges :** • 4 clock domains for functional mode and single clock-do mode. • The design included 16 corners for functional and DI • Rectilinear floorplan with lots of congestion and util 75%. • Timing closure across different corners.		
Technologies	TSMC 65nm Generic Superb		

Technologies	45nm 65nm Generic Superb
Tools	IC Compiler, Calibre
Key Achievements	Quick Turn-around time

Project 5:

Project Name	iMX-508	Duration	2 Months

Name: **XXXXXXXX**

		Team Size	3
Description	IMX.508 is an application processor used in eReader devices. The operating frequency of the chip is 400MHz with specific domains operating up to 800MHz. The design involved Cortex ARM A8 processors, Electronic paper display (EPD) controller etc. The design was targeted to 65**nm** CMOS process and Crolles foundry. The size of the chip is 5.6x5.8mm.		
Role& Contribution	**Role:** Physical Verification **Description & Challenges :** • Involved in the porting of the chip from Customer specific tool to Cadence Virtuoso including Technology file creation etc. • Porting of customer specific Physical verification flow to L&T specific flow for sign-off • DRC, LVS and Antenna fix and sign-off for the full-chip.		
Technologies	Crolles 65nm		
Tools	Calibre		
Key Achievements	Creation and verification of chip using Virtuoso flow. Customer sign-off flow was different.		

Project 6:

Project Name	ARM Hardening	Duration	2 Months
		Team Size	1
Description	ARM hardening is processor core with the Die size of 2.5x2.6mm. The Gate-count of the chip including Memories and macros was around 14M and it had around 21 macro instances. This was implemented at 40nm technology.		
Role& Contribution	**Role:** Place and Route, STA **Description & Challenges :** • The operating frequency of the chip was 600MHz. • The timing closure was done for 2 modes and 4 corners. MMMC was used for timing closure during Place and route. • LVT cells were used for Leakage optimization along with Clock-gating. • 15 clock domains for functional mode and single clock-domain for DFT mode.		

Name: **XXXXXXXX**

Technologies	TSMC 40nm
Tools	IC Compiler, PT
Key Achievements	Good customer appreciation

Project 7:

Project Name	Automotive SoC (Different Versions)	Duration	15 Months
		Team Size	5
Description	Full-chip physical design implementation of an Automotive SoC targeted to low power applications. The Gate-count of the chip excluding Memories and macros was around 4M and it had around 74 macro instances. This was implemented at 90nm technology. The operating frequency of the chip was 160MHz. The Size of the chip is 7.07x9.05mm.		
Role& Contribution	**Role:** IO Plan, Power Route, Floorplan, DRC& LVS **Description & Challenges :** • Power switches were used in the design. • Floor planning and power planning were done based on the power-domains. • This chip was implemented using the Common Power Format (CPF) flow.		
Technologies	90nm Fujitsu Foundry		
Tools	SoC Encounter, Calibre, Lavis		
Key Achievements	Lot of customer appreciation and quick turn-around		

Educational Qualification & Certifications

M.Tech	VLSI, Sathyabama University, Chennai completed in 2006
	2004

Training and Seminars

Name: **xxxxxxxx**

- Attended Tool trainings from Cadence, Mentor and Synopsys
- Attended tool update training from EDA vendors
- Attended Webinar of various Physical Design topics

##

RESUME
XXXXXXXXXX XXXXXXXXX

Xxxxxxxxx **Mobile:** 91-xxxxxxxx

Email: xxxxxxx@gmail.com

CAREER OBJECTIVE

Intend to build a career with committed and dedicated people, which will help me to realize my potential, enhance my skill set in the field of High speed VLSI Physical design and help the organization grow.

INDUSTRIAL EXPERIENCE

- **CYIENT(InfoTech Enterprises) Ltd, Hyderabad (ASIC Physical Design Group)**

  Designation: Senior Physical Design Engineer
  Duration: from 01st July **2011** to till date**.**

SUMMARY

- Experience in handling High utilized and critical blocks.
- Experience in Physical Design for 45nm and 32nm Technologies using IBM and Cadence Tools.
- Worked on Physical Design flow stages like **Floor planning**, **Place and Route**, **CTS**, **Timing Analysis**, **SI Analysis**, **IR Drop Analysis**, **DRC\LVS**.
- Block level **Timing Closure** and **Multi Voltage Design**. Resolving various **Block level** PnR issues.
- Expertise in Scripting Skills.
- Highly adaptable to all kinds of environment.
- Always on the look to improve skills and grow with the organization.

SKILL SET

Floor Plan & PNR - IBM Chipbench, SOC Encounter
Timing Analysis - Einstiemer, ETS and Prime Time

1

RESUME
XXXXXXXXXX XXXXXXXXX

Synthesis - RC compiler
Physical Verification - Buldozer, Calibre
RC-Extraction - QRC and Star RC
IRDROP - Redhawk
Scripting Languages - TCL/TK, PERL

EDUCATION

- M.Tech in Digital Systems & Signal Processing from GITAM University Vishakapatnam with an aggregate of 79.0% (2009 to 2011)
- B.Tech in Electronics & Communication Engineering from JNTU Hyderabad with an aggregate of 63.0% (2005 to 2009)
- Intermediate from Board of Intermediate Education, Hyderabad with an aggregate of 88.3% (2003 to 2005)
- X class from Board of SSC with 82 % (2002 to 2003)

Projects Undertaken at Infotech Enterprises

PROJECT - 1

BLOCK 1

Technology/ Layers : **32nm**
Tools used : ChipBench, ChipEdit, Einstiemer & Buldozer.
Gate count : 2M
Hard Macros : 70
Frequency : 1 GHz
Clocks : 3
Role& responsibilities : Block level physical design

- Block level Floorplanning, Power planning, DeCap insertion, Placement Driven synthesis, Post placement Timing closure, Clock Tree Synthesis, Clock wiring, Post clock Timing closure, clock slew fixing, late mode and Early mode optimization, Timing driven and SI driven Routing, Post Route Timing Fixing, Fixing DRCs.

BLOCK 2

Technology/ Layers : **32nm**
Tools used : ChipBench, ChipEdit, Einstiemer & Buldozer.

2

RESUME
XXXXXXXXXX XXXXXXXXX

Gate count : 1.6M
Hard Macros : 90
Frequency : 1 GHz
Clocks : 3
Role& responsibilities : Block level physical design

- Block level Floorplanning, Power planning, DeCap insertion, Placement Driven synthesis, Post placement Timing closure, Clock Tree Synthesis, Clock wiring, Post clock Timing closure, clock slew fixing, late mode and Early mode optimization, Timing driven and SI driven Routing,Post Route Timing Fixing, Fixing DRCs.

PROJECT - 2

BLOCK 1

Technology/ Layers : **45nm**
Tools used : ChipBench, ChipEdit, Einstiemer & Buldozer.
Gate count : 1M
Hard Macros : 80
Frequency : 500 MHz
Clocks : 5
Role& responsibilities : Block level physical design

- Block level Floorplanning, Power planning, DeCap insertion, Placement Driven synthesis, Post placement Timing closure, Clock Tree Synthesis, Clock wiring, Post clock Timing closure, clock slew fixing, late mode and Early mode optimization, Timing driven and SI driven Routing, Post Route Timing Fixing, Fixing DRCs.

BLOCK 2

Technology/ Layers : **45nm**
Tools used : ChipBench, ChipEdit, Einstiemer & Buldozer.
Gate count : 700K
Hard Macros : 130
Frequency : 500 MHz
Clocks : 5
Role& responsibilities : Block level physical design

- Block level Floorplanning, Power planning, DeCap insertion, Placement Driven synthesis, Post placement Timing closure, Clock Tree Synthesis, Clock wiring, Post clock Timing closure, clock slew fixing, late mode and Early mode optimization, Timing driven and SI driven Routing, Post Route Timing Fixing, Fixing DRCs.

RESUME
XXXXXXXXXX XXXXXXXXX

PROJECT - 3

BLOCK 1

Technology/ Layers : **65nm**
Tools used : SOC Encounter, ETS & PVS.
Gate count : 1.8M
Hard Macros : 20
Frequency : 700 MHz
Clocks : 3
Role& responsibilities : Block level physical design

- Floor Planning & Placement, Pre-CTS Optimization, Clock Tree Synthesis, Post CTS Optimization, SI Driven Routing, RC Extraction, STA & Post route Optimization, DRC, LVS, Antenna checks

BLOCK 2

Technology/ Layers : **65nm**
Tools used : SOC Encounter, ETS & P\
Gate count : 520K
Hard Macros : 30
Frequency : 700 MHz

Frequency : 700 MHz
Clocks : 3
Role& responsibilities : Block level physical design

- Floor Planning & Placement, Pre-CTS Optimization, Clock Tree Synthesis, Post CTS Optimization, SI Driven Routing, RC Extraction, STA & Post route Optimization, DRC, LVS, Antenna checks

AWARDS AND CERTIFICATES

- Has given a seminar on "ANALYSIS OF SPEECH PROCESSING TECHNIQUES " in the proceedings of National Conference on Electronic Circuits and Communication Systems, held on 12st APRIL 2011.

PERSONAL PROFILE

Father's Name :
Date of Birth :
Gender :

RESUME
XXXXXXXXXX XXXXXXXXX

Marital Status :
Nationality :
Linguistic knowledge :
Alternate Email Id :
Permanent address :

DECLARATION

I here by declare that all the particulars furnished above are authentic to best of my knowledge and belief.

Place:
(xxxxxxxxxxxxx)

5

##

XXXXXXXX
Contact No : +91-xxxxxxx
Email ID : xxxxxxxxx@gmail.com

CAREER OBJECTIVE

To secure a challenging position in an esteemed organization that gives ample scope to fulfill professional and personal goals and to work for development of organization to the highest possible limit.

WORKING EXPERIENCE

- Presently working as a **Physical Design Engineer** in **Infotech Enterprises Ltd** from Dec 2010 in Visakhapatnam.

PROFESSIONAL BACKGROUND

- **2.9** years of Experience in **ASIC** Design Field.
- Experience in lower design nodes and **various design technologies** like **40**nm, **65**nm, **90**nm, **130**nm and **180**nm.
- Has Expertise in Physical Design flow stages like Floor planning, Placement, CTS, Timing Closure, SI analysis, IR drop analysis, DRC/LVS and ECO's (Functional and Metal).
- Block level timing closure and PV closure. Resolving various block level P&R issues.
- Hands on experience on **various EDA tools**.
- Ability to work independently as well as part of team.
- Good Analytical, design and problem solving skills.

ACADEMICS

- **B.Tech** in **Electronics & Communication Engineering** affiliated from **JNTU-K** in year 2010 with 70%.
- **Intermediate** in **MPC** from **Modern junior college** in year 2006 with 88.7%.
- **SSC** in **Mathematics & Science** from **Modern high school** in year 2004 with 82%

TECHNICAL SKILLS

Place & Routing	: SOC Encounter
Static- timing Analysis	: PTSI, ETS
RC Extraction	: Qrc
Signal Integrity	: Prime Time –SI
IR Drop Analysis	: Vstorm
Physical verification	: Calibre (DRC, LVS, ANTENNA, ERC), PVS
Gds to Def conversion	: Virtuoso
Scripting Language	: Tcl, Shell

PROJECT DETAILS

BLOCK 1:

Technology/Layers : 40nm/9
Tools used : SOC Encounter, Calibre, Vstorm, QRC, PTSI.
Gate count : 3.12 M
Hard Macros : 49
Frequency : 666.67 MHz, 531.91 MHz, 269.53 MHz, 166.67 MHz
Clocks : 10
Role & Description : Block level physical design

- The tasks handled were Floor planning, Place & Route of the design, perform STA and bring the block to timing closure, Clean DRC/LVS issues at block level.
- Basically the block is timing and congestion critical. Floorplan has become major thing for better QOR. Performed so many Floorplan experiments to arrive at a better floorplan. Criticality faced while meeting the clock latency.

BLOCK 2:

Technology/Layers : 90nm/4
Tools used : SOC Encounter, Calibre, Vstorm, QRC, PTSI.
Gate count : 25K
Hard Macros : 4
Frequency : 4 MHz
Clocks : 2
Role & Description : Block level physical design

- The tasks handled were GDS to DEF conversion, Floor planning, Place & Route of the design, perform STA and bring the block to timing closure, Clean DRC/LVS issues at block level, Metal Layer ECO's.
- Basically the block is congestion critical. Criticality faced while meeting the clock latency, and clearing the DRC/ANTENNA violations in Metal Layer ECO stage.

BLOCK 3:

Technology/Layers : 130nm/4
Tools used : SOC Encounter, Calibre, Vstorm, QRC, PTSI.
Gate count : 13K
Hard Macros : 4
Frequency : 4 MHz
Clocks : 2
Role & Description : Block level physical design

- The tasks handled were Floor planning, Place & Route of the design, perform STA and bring the block to timing closure, Clean DRC/LVS issues at block level.
- Basically the block is congestion critical. Criticality faced while meeting the clock latency and clearing the DRC.

BLOCK 4:

Technology/Layers : 65nm/7
Tools used : SOC Encounter, Calibre, Vstorm, QRC, PTSI.
Gate count : 1.8 M
Hard Macros : 20
Frequency : 900MHz
Clocks : 3
Role & Description : Block level physical design

- Basically the block is timing and congestion critical. Floorplan has become major thing for better QOR. Performed so many Floorplan experiments to arrive at a better floorplan.
- The tasks handled were Floor planning, Place & Route of the design, perform STA and bring the block to timing closure, Clean DRC/LVS issues at block level.

BLOCK 5:

Technology/Layers : 130nm/5
Tools used : SOC Encounter, PVS, ETS.
Gate count : 300k
Hard Macros : 12
Frequency : 200MHz
Clocks : 17
Role : Block level physical design

- Basically the block is timing critical. Working with multiple clocks. C
meeting the clock latency.
- The tasks handled were Floor planning, Place & Route of the design, perform STA and bring the

block to timing closure, Clean DRC/LVS issues at block level.

BLOCK 6:

Technology/Layers : 180nm/3
Tools used : SOC Encounter, PVS, ETS.
Gate count : 110k
Hard Macros : 12
Frequency : 150MHz
Clocks : 3
Role & Description : Block level physical design

- This is my first real time block, No criticality in Timing or floorplan.
- The tasks handled were Floor planning, Place & Route of the design, perform STA and bring the block to timing closure, Clean DRC/LVS issues at block level.

Awards & Certifications

- Achieved "Team of the Month" for the month Nov 2012, for last Project.
- Pat on the back from the manager.

PERSONAL INFORMATION

Full Name :
Father's Name :
Nationality :
Sex :
Marital Status :
Date of Birt :
Present Address :

DECLARATION

I hereby declare that all the above information is true and correct to the best of my knowledge and belief.

Place:

Date: (xxxxxxxxxxx.)

XXXXXXX XXXXXX E-MAIL:
xxxxxxx**@gmail.com**
M.Tech with 4 years of Physical Design Experience Mobile No. :
+91-xxxxx

CAREER OBJECTIVE

To excel in the field of VLSI Technology and to work in an innovative and competitive world.

PROFESSIONAL SUMMARY

• Over 4 years of experience primarily in ASIC Physical Design .

• Good Experience in all aspects of ASIC design including floor planning, power planning ,
IR drop analysis ,clock tree synthesis, place and route, signal integrity analysis and repair ,
Static Timing Analysis and physical verification .

• Worked on 28nm & 20nm process node designs at **Texas Instruments** as a Physical design Engineer(Consultant) .

• Strong Experience with EDA tools like Cadence EDI (SOC Encounter) , Encounter Timing
System , Synopsys Prime Time ,Caliber & RTL Compiler.

• Worked on ASIC Physical design flow in 20nm, 28nm,40nm, 65nm, 90nm and 130nm
technologies.

• Proficient in script writing in TCL, Perl and Unix/Linux environment.

• Worked on Cadence Low Power (CPF) flow - Power Shutoff Methodology .

•Practical Knowledge in Hierarchical Partitioning & design with Multi-Supply voltage(MSV)

EXPERIENCE SUMMARY

- Working as Physical Design Engineer in First Pass Semiconductors Pvt Ltd. (Since June 2011 to till date).
- Worked as a Design Engineer in Cybermate Infotek P Ltd. (Since July 2010 to May 2011).

TECHNICAL EXPERTISE

- EDA Tools : Cadence EDI , RTL Compiler, ETS, Magma Talus Synopsys Prime Time -SI , Calibre ,Virtuoso & Assura.
- HDL Languages : VHDL, Verilog
- Scripting Language : TCL , Shell ,PERL
- Programming Languages : C, C++
- Operating Systems : MS-DOS, Windows, Linux

PROJECT DETAILS

Texas Instruments (Client) : Sep 2011 - Dec 2

1. Implementations of multimillion gate complexity & 28 nm Design node

Worked on timing critical and congestion blocks. Responsibilities were doing Floor planning, IO planning, Power Routing, Placement, Clock

were doing Floor planning, IO planning, Power Routing, Placement, Clock tree Synthesis, Routing, RC Extraction and Static Timing Analysis.

Project Name: OMAP5432

No of Blocks Handled : 3 - IDDS , ECD & IME3
Tools : Cadence EDI , QRC & PT -SI.
Technology : 28 nm
Macros : 12
Instance Count : ~ 0.3 M
No of Clocks & Frequency : 3 - 5 clocks & 500MHz – 1 Ghz
Role : Netlist to GDSII (Challenging Floorplan & timing closure responsible for block level timing with SI

2. **Power Performance Area (PPA) Enhancements for 20 nm Designs**
   Enhancement of PPA for 20 nm designs at routing as well as Pre-routing stage by use of different methodologies such as Structured Data Path , Redundant Via Insertion , LVT cells insertion

• By analyzing criticality of the design, introduced Structured Data Paths (SDP) for Registers and NDR for critical nets

• Responsible for bringing up best styles of introduction of LVT cells & Redundant Via Insertion at appropriate Routing stage

3. **Validation & Comparison of Technology Library for 20 nm design Node**
   Responsible for (a) Bringing up the best combination of routing Pitches for layer stacks for better routability in 20 nm design node (b) Delay comparison (both net and cell) for each layer stacks for 1mm lengths (c) Validated and compared technology LEF for future generation chips

4. **Worked on Cadence EDI tool evaluation for its SDP features**

5. **Developed & Implemented flow using TCL & dbCommands for sweeping around critical nets for finding out vacant routing tracks in EDI database**

➢ First Pass Semiconductors Pvt Ltd :

Project Name: (TCPCI4A CHIP)

Objective : Chip level implementation with Flip chip Technology
Tools : RTL compiler , Cadence EDI ,ETS , PVS & Calibre .
Gate count/Area : 5 M
Digital Blocks : 3
Macros : 2
No. of Clocks : 20
Frequency : 800MHz
Technology/Layers : GF 40nm LP / 7 Metal Layers

Roles and Responsibilities

Synthesis
• Synthesized three digital blocks which are instantiated inside Analog block and top level RTL with scan insertion after finding out the maximum frequency c
• Developed Design constraints (SDC) for chip & block lev

FloorPlanning
• Estimated area of the chip and Placed IOs along the side edges .
• Power planning & IR drop analysis for entire chip .

Added Endcap & tap cells as per Foundry requirements
• Created and assigned Bumps over core area and routed the flip chip connectivity's.

Placement ,CTS & Routing
• Placement with guides for meeting timing criticality

• Clock Tree Synthesis with anchor buffers and NDR
• ECO fixes after routing by considering Xtalk issues.

STA
• Created timing library for all three digital blocks and integrated as one for Chip level timing analysis.
• Analyzed timing reports in OCV mode
• Setup & hold Analysis on Function & scan mode
• SPEF extraction for multicorners and timing analysis for all corners including cross corners also.

Physical Verification & Package
• DRC & LVS for block and chip level .
• Derived the package co-ordinates after verifying the bump placements of Analog macros by aligning extra bumps over it and doing final DRC & LVS check
• DRC+ (pattern matching) check for entire chip .
• Compared the Tapeout GDS & Extra bump inserted GDS for finding any mismatches in bump alignment by using fastXOR in PVS tool.

Project Name: RS9116 (Low power Design)

Objective : Block level place and route
Tools : Cadence EDI , Vstorm , QRC , ETS.
Technology : GF 40nm
Block Details Methodolgy : Low Power implementation with PSO
Gate Count : 2.5 M
Macros : 33
No. of clocks & Frequency : 5 & 333MHz
Roles and Responsibilities : CPF creation as per design specs , Floorplanning including Power Switch Insertion , IR drop Analysis ,challenging CTS (using anchor buffers) , timing closure with SI.

Project Name: Cipher

Tools : Cadence EDI , Vstorm , QRC , ETS & Caliber.
Technology : TSMC 65nm
Gate Count : 1.1M
Macros : 4
No. of clocks & Frequency : 3 & 300MHz

Roles and Responsibilities : Floorplan ,IR drop Analysis ,challenging CTS (using anchor buffers) , timing closure with SI , DRC and LVS .

Project Name: Mac_Core

Tools : Cadence EDI , Vstorm , QRC, ETS & Assura .
Technology : 90nm

Gate Count : 1.2M
Macros : 7
No. of clocks & Frequency : 4 & 125MHz
Roles and Responsibilities : challenging Floorplan & timing closure responsible for block
Level timing, power planning ,DRC & LVS.

Project Name: amba_usb

Tools : SOC Encounter QRC, ETS & Virtuoso & Assura .
Technology : 130nm
Gate Count : ~1M
Macros : 10
No. of clocks & Frequency : 3 & 111MHz
Roles and Responsibilities : Floorplan & timing closure responsible for block
Level timing, DRC & LVS.

Project Name: DMA

Objective : Block level place and route
Tools : SOC Encounter,RTL Compiler, QRC, ETS
Technology : 130nm
Gate Count : ~1M
Macros : 5
No. of clocks & Frequency : 5 & 100MHz
Roles and Responsibilities : Synthesis , Floorplan & Power planning ,timing closure responsible for block Level timing.

ACADEMIC QUALIFICATIONS

M.Tech (2008-2010) in VLSI Design form Amrita Vishwavidyapeetham with CGPA of 8.24

B.Tech (2004-2008) in Electronics and Communication from Cochin University of Science & Technology with 66.3 %

Higher Secondary from Board of Higher Secondary,Kerala with 84.5%

SSLC from state board Kerala with 90.16%

ACHIEVEMENTS

- Organizing committee member of 'INCENDIO', a South Indian Technical Festival organized by ECE Dept of College of Engineering Thalassery.
- 'A' certificate in NCC.

STRENGHTS

- Mindset to help others and understand them
- Quick Learner, Self motivated and the zeal to work in a team
- Highly promising, sincere, ambitious and smart working.

PERSONAL DETAILS

Age & DOB :
Father's Name :
Marital status :
Nationality :
Languages known :
Hobbies :
Address :

DECLARATION

I here by declare that all information provided above is true to the best of my Knowledge.

Place:
xxxxxxxxxxxxx

VLSIGuru is a top VLSI training Institute based in Bangalore. Setup in 2012 with the motto of 'quality education at affordable fee' and providing 100% job oriented courses.

NAVIGATIONS

- E-Learning
- FAQ's
- Corporate Training
- Contact Us
- Course Enroll
- Installment Form
- Important Links

SUPPORT

- Internship Request
- Course Registration
- Training Overview
- Certificate Request
- Course Feedback
- Course Schedule
- Mock Interview

OUR COURSES

- Functional / ASIC verification
- RTL design and integration
- Design for testability (DFT)
- Custom and Analog Layout
- Synthesis and STA
- IR Drop analysis using RedHawk
- Custom/Analog layout

OUR COURSES

Course Registration

Physical Design

Functional verification

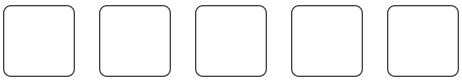
Physical verification

FPGA system design

Embedded systems

PERL Training

Physical Design



Go To Top

Course Registration